

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of the claims in the application:

Claim 1. (Currently Amended) A semiconductor memory device of a dynamic type for refreshing information stored in a memory space, so as to hold the information continuously by amplifying the information stored in said memory space to rewrite the amplified information in said memory space, said memory device comprising:

a refresh control circuit for performing refreshment of the information only to a submemory space, which is in use when the refreshment of the information is performed, said submemory space holding the information necessary to be refreshed, selected from among a plurality of submemory spaces formed by a previous division of said memory space,

wherein said refresh control circuit performs a logical product of data pertaining to whether each of said submemory spaces are in use and refresh address data to be input to each address, and performs control of whether said refreshment is performed or not to each submemory space with said refresh circuit based on a result of said logical product.

--2. (Currently Amended) A semiconductor memory device of a dynamic type including a memory cell array for storing information, and a refresh circuit for refreshing the information stored in said memory cell array, so as to hold

the information continuously, by amplifying the information stored in said memory cell array to rewrite the amplified information in said memory cell array, said memory device comprising:

a refresh control circuit for controlling an operation of said refresh circuit so as to perform refreshment of the information only to a submemory space that is in use when the refreshment of the information is performed, said submemory space holding the information necessary to be refreshed, among a plurality of submemory spaces formed by previous division of an address space in a memory space of said memory cell array,

wherein said refresh control circuit performs a logical product of data pertaining to whether each of said submemory spaces are in use and refresh address data to be input to each address, and performs control of whether said refreshment is performed or not to each submemory space with said refresh circuit based on a result of said logical product.

--3. (Canceled)

--4. (Currently Amended) The A semiconductor memory device according to claim 2, of a dynamic type including a memory cell array for storing information, and a refresh circuit for refreshing the information stored in said memory cell array, so as to hold the information continuously, by amplifying the information stored in said memory cell array to rewrite the amplified information in said memory cell array, said memory device comprising:

a refresh control circuit for controlling an operation of said refresh circuit so as to perform refreshment of the information only to a submemory space that is in use when the refreshment of the information is performed, said submemory space holding the information necessary to be refreshed, among a plurality of submemory spaces formed by previous division of an address space in a memory space of said memory cell array,

wherein said memory cell array includes a row decoder, and said row decoder is set to specify a row address to which said refreshment is performed in addresses of said memory cell array, and wherein said refresh control circuit is inserted between said memory cell array and said row decoder, said refresh control circuit being set to intervene in a function of said row decoder for specifying the row address to which said refreshment is performed so as to control whether said refreshment is performed to each of said submemory spaces.

--5. (Currently Amended) The semiconductor memory device according to claim 2, of a dynamic type including a memory cell array for storing information, and a refresh circuit for refreshing the information stored in said memory cell array, so as to hold the information continuously, by amplifying the information stored in said memory cell array to rewrite the amplified information in said memory cell array, said memory device comprising:

a refresh control circuit for controlling an operation of said refresh circuit so as to perform refreshment of the

information only to a submemory space that is in use when the refreshment of the information is performed, said submemory space holding the information necessary to be refreshed, among a plurality of submemory spaces formed by previous division of an address space in a memory space of said memory cell array,

wherein said memory cell array includes a row decoder, and said row decoder is set to specify a row address to which said refreshment is performed in addresses of said memory cell array, and wherein said refresh control circuit is provided in said row decoder, said refresh control circuit being set to intervene in a function of said row decoder for specifying the row address to which said refreshment is performed so as to control whether the refreshment is performed to each of said submemory spaces.

--6. (Previously Presented) The semiconductor memory device according to claim 2, wherein said memory cell array includes a row decoder and a refresh address counter, and said row decoder and said refresh address counter are set to specify a row address to which said refreshment is performed in addresses of said memory cell array, and wherein said refresh control circuit is attached to said refresh address counter, said refresh control circuit being set to intervene in a function of said refresh address counter for outputting the row address to which said refreshment is performed so as to control whether the refreshment is performed to each of said submemory spaces.

--7. (Previously Presented) The semiconductor memory device according to claim 2, wherein said memory cell array includes a row decoder and a refresh address counter, and said row decoder and said refresh address counter are set to specify a row address to which said refreshment is performed in addresses of said memory cell array, and wherein said refresh control circuit is provided inside said refresh address counter, said refresh control circuit being set to intervene in a function of said refresh address counter for outputting the row address to which said refreshment is performed so as to control whether the refreshment is performed to each of said submemory spaces.

--8. (Previously Presented) The semiconductor memory device according to claim 2, further comprising a row decoder, a multiplexer and a refresh address counter connected in order to said memory cell array, and said row decoder, said multiplexer and said refresh address counter are set to specify a row address to which said refreshment is performed in addresses of said memory cell array, and wherein said refresh control circuit is inserted between said refresh address counter and said multiplexer, said refresh control circuit being set to intervene in a refresh address counter's output of the row address to which said refreshment is performed, the output being transmitted to said row decoder through said multiplexer, so as to control whether the refreshment is performed to each of said submemory spaces.

--9. (Previously Presented) The semiconductor memory device according to claim 2, further comprising a row decoder, a multiplexer and a refresh address counter connected in order to said memory cell array, and said row decoder, said multiplexer and said refresh address counter are set to specify a row address to which said refreshment is performed in addresses of said memory cell array, and wherein said refresh control circuit is provided inside said multiplexer, said refresh control circuit being set to intervene in a refresh address counter's output of the row address to which said refreshment is performed, the output being transmitted to said row decoder through said multiplexer, so as to control whether the refreshment is performed to each of said submemory spaces.

--10. (Currently Amended) The semiconductor memory device according to claim 2, wherein said memory space is divided into a plurality of ~~memory~~ information spaces to store respective kinds of contents of information different from one another, and at least one of said plurality of ~~memory~~ information spaces is further divided into said plurality of submemory spaces.

--11. (Currently Amended) A refresh control circuit for a semiconductor memory device of a dynamic type for refreshing information stored in a memory space, so as to hold the information continuously, by amplifying the information stored

in said memory space to rewrite the amplified information in said memory space,

wherein said refresh control circuit performs control of refreshment of the information only to a submemory space, which is in use when the refreshment of the information is performed, said submemory space holding the information necessary to be refreshed, selected from among a plurality of submemory spaces formed by a division of said memory space, and

wherein said refresh control circuit performs a logical product of data pertaining to whether each of said sub memory spaces are in use and refresh address data to be input to each address, and performs control of whether said refreshment is performed to each submemory space with said refresh circuit based on a result of said logical product.

--12. (Currently Amended) A refresh control circuit for a semiconductor memory device of a dynamic type including a memory cell array for storing information and a refresh circuit for refreshing the information stored in said memory cell array, so as to hold the information continuously, by amplifying the information stored in said memory cell array to rewrite the amplified information in said memory cell array,

wherein said refresh control circuit controls an operation of said refresh circuit so as to perform refreshment of the information only to a sub memory space which is in use when the refreshment of the information is performed, said sub

submemory space, holding the information necessary to be refreshed, said submemory space being selected from among a plurality of sub memory spaces formed by previous division of an address space in a memory space of said memory cell array-
,and

wherein said refresh control circuit performs a logical product of data pertaining to whether each of said sub memory spaces are in use and refresh address data to be input to each address, and performs control of whether said refreshment is performed to each submemory space with said refresh circuit based on a result of said logical product.

--13. (Canceled)

--14. (Currently Amended) The refresh control circuit according to claim 12, wherein said memory space is divided into a plurality of ~~memory~~ information spaces to store respective kinds of contents of information different from one another, and at least one of said divided ~~memory~~ information spaces is further divided into said plurality of submemory spaces.

--15. (Currently Amended) A method for refreshing storage in a semiconductor memory device of a dynamic type for refreshing information stored in a memory space, so as to hold the information continuously, by amplifying the information stored in said memory space to rewrite the amplified information in said memory space, said method comprising the

steps of:

dividing said memory space into a plurality of submemory spaces; and

performing refreshment of the information only to a selected submemory space among the plurality of submemory spaces, said selected submemory space being in use when the refreshment of the information is performed, said submemory space holding the information necessary to be refreshed-, and

performing a logical product of data pertaining to whether each of said sub memory spaces is in use and refresh address data to be input to each address, wherein control of whether said refreshment is performed to each submemory space is performed based on a result of said logical product.

--16. (Currently Amended) A refresh method for refreshing information stored in a memory cell array, so as to hold the information continuously, by amplifying the information to rewrite the amplified information in said memory cell, said memory cell array being provided in a semiconductor memory device of a dynamic type, said method comprising the steps of:

dividing an address space in a memory space of said memory cell array into a plurality of submemory spaces; and

performing refreshment of the information only to a selected submemory space among the plurality of submemory spaces, said selected submemory space being in use when the refreshment of the information is performed, said submemory space holding the information necessary to be refreshed-, and

performing a logical product of data pertaining to whether each of said sub memory spaces is in use and refresh address data to be input to each address, wherein control of whether said refreshment is performed to each submemory space is performed based on a result of said logical product.

--17. (Canceled)

--18. (Currently Amended) The refresh method according to claim 16, wherein said memory space is divided into a plurality ~~memory~~ information spaces to store respective kinds of contents of information different from one another, and at least one of said divided ~~memory~~ information spaces is further divided into the plurality of submemory spaces to perform control of said refreshment of the information to each of said submemory spaces.